

CLAIMS

What is claimed is:

- 1 1. A system for implementing vertical threading in a processor, comprising:
2 a header block that receives a multi-function signal and generates a
3 plurality of signals using the multi-function signal; and
4 a data storage block that is responsive to the plurality of signals
5 generated by the header block.
- 1 2. The system of claim 1, wherein the header block comprises header circuitry
2 which distinguishes between different functionalities exhibited by the
3 multi-function signal.
- 1 3. The system of claim 1, wherein the multi-function signal comprises a scan
2 enable function, a clock enable function, and a clock disable function.
- 1 4. The system of claim 1, wherein the header block receives signals in
2 addition to the multi-function signal.
- 1 5. The system of claim 4, wherein the additional signals received by the
2 header block comprise a clock input signal and a global thread identifier
3 signal.
- 1 6. The system of claim 5, wherein the global thread identifier signal is used by
2 the processor to selectively indicate to the header block that the data storage
3 block needs to switch process threads.

- 1 7. The system of claim 5, wherein the clock input signal is generated by the
2 processor and is used by the header block to determine time references for
3 operations in the header block.
- 1 8. The system of claim 1, wherein the plurality of signals generated by the
2 header block comprise an external pulse signal, an inverted external pulse
3 signal, a scan clock signal, and a local thread identifier signal.
- 1 9. The system of claim 8, wherein the external pulse signal is used by the data
2 storage block as a time reference for operations in a normal mode.
- 1 10. The system of claim 8, wherein the inverted external pulse signal is an
2 inverse of the external pulse signal, and wherein the inverted external pulse
3 signal is used by the data storage block to facilitate operations in a normal
4 mode.
- 1 11. The system of claim 8, wherein the scan clock signal is used by the data
2 storage block as a time reference for operations in a scan mode.
- 1 12. The system of claim 8, wherein the local thread identifier signal is
2 generated by the header block using a global thread identifier signal.
- 1 13. The system of claim 1, wherein the data storage block receives the plurality
2 of signals generated by the header block, and wherein the header block and
3 the data storage block are part of a multiple-bit flip-flop, and wherein the
4 multiple-bit flip-flop is used in a processor pipeline.

- 1 14. The system of claim 13, wherein the processor pipeline comprises a
2 plurality of multiple-bit flip-flops.
- 1 15. The system of claim 1, wherein the data storage block comprises at least
2 one data storage element that is capable of storing data for a plurality of
3 process threads.
- 1 16. The system of claim 1, wherein the header block controls a plurality of
2 modes in which the data storage block may operate, and wherein the multi-
3 function signal comprises additional functions.
- 1 17. A method for implementing vertical threading, comprising:
2 receiving a multi-function signal in a header block;
3 determining which function the multi-function signal serves;
4 generating signals within and from the header block according to the
5 determination; and
6 operating a multiple-bit flip-flop in one of a plurality of operation
7 modes dependent upon the determination of which function
8 the multi-function signal serves.
- 1 18. The method of claim 17, wherein the multi-function signal can serve as a
2 scan enable function, a clock enable function, and a clock disable function.
- 1 19. The method of claim 17, wherein the signals generated from the header
2 block are received by a data storage block.

- 1 20. The method of claim 19, wherein the data storage block operates in one of
2 the plurality of operation modes dependent upon the signals generated from
3 the header block.
- 1 21. The method of claim 17, wherein the determination of which mode to
2 operate the multiple-bit flip-flop comprises:
3 distinguishing between multiple characteristics of the multi-function
4 signal;
5 using the multi-function signal to generate intermediary signals; and
6 using the intermediary signals to determine when the multiple-bit
7 flip-flop should go into or remain in one of the plurality of
8 operation modes.
- 1 22. The method of claim 21, wherein the intermediary signals are internal to
2 the header block, and wherein the plurality of operation modes comprise a
3 normal mode and a scan mode.
- 1 23. The method of claim 18, wherein the determination that the multi-function
2 signal serves as the scan enable function indicates that the multiple-bit flip-
3 flop should operate in a scan mode, and wherein the determination that the
4 multi-function signal serves as the clock enable function indicates that the
5 multiple-bit flip-flop should operate in a normal mode.
- 1 24. The method of claim 18, wherein the determination that the multi-function
2 signal serves as the clock disable function indicates that the multiple-bit
3 flip-flop should temporarily suspend normal mode data operations for
4 alignment purposes.

1 25. The method of claim 17, further comprising:
2 inputting a first clock signal;
3 inputting the multi-function signal;
4 inputting a global thread identifier signal; and
5 selectively generating an external pulse signal, a scan clock signal,
6 and a local thread identifier signal dependent upon the
7 behavior of the pulse signal, the multi-function signal, and the
8 global thread identifier signal.

1 26. The method of claim 25, further comprising:
2 generating an internal pulse signal using the first clock signal; and
3 using the internal pulse signal to activate the external pulse signal
4 when the multi-function signal serves as a clock enable
5 function.

1 27. The method of claim 25, further comprising:
2 deactivating the external pulse signal when the multi-function signal
3 begins to serve as a scan enable function.

1 28. The method of claim 25, further comprising:
2 activating the external pulse signal at an end of a clock cycle in
3 which the multi-function signal begins to serve as a scan
4 enable function when the multi-function signal begins to
5 serve as a clock enable function before the end of the clock
6 cycle.

1 29. The method of claim 25, further comprising:

2 deactivating the external pulse signal when the multi-function signal
3 serves as a scan enable function for more than one clock
4 cycle.

1 30. The method of claim 27, wherein the multiple-bit flip-flop operates in a
2 scan mode when the multi-function signal serves as the scan enable
3 function for more than one cycle.

1 31. The method of claim 30, further comprising:
2 activating the scan clock signal when the multiple-bit flip flop is in
3 the scan mode.

1 32. The method of claim 25, further comprising:
2 deactivating the external pulse signal when the global thread
3 identifier signal toggles;
4 selectively generating the local thread identifier signal when the
5 global thread identifier signal toggles; and
6 activating the external pulse signal at an end of a clock cycle in
7 which the global thread identifier signal toggled.

1 33. The method of claim 25, wherein the external pulse signal, the scan clock
2 signal, and the local thread identifier signal are received by the data storage
3 block, and wherein additional signals are selectively generated to the data
4 storage block.

1 34. The method of claim 25, wherein the multiple-bit flip-flop operates in a
2 normal mode when the external pulse signal is activated.

1 35. The method of claim 17, further comprising:
2 converting an existing processor without vertical threading into a
3 processor with vertical threading without changing an
4 architectural layout of the existing processor.

1 36. An apparatus for implementing a vertical threading scheme, comprising:
2 means for inputting a clock signal;
3 means for inputting a multi-function signal;
4 means for inputting a global thread identifier signal;
5 means for distinguishing between different functionalities of the
6 multi-function signal to determine which of a plurality of
7 functions the multi-function serves; and
8 means for generating a plurality of signals based on the
9 determination of which of the plurality of functions the multi-
10 function serves, the clock signal, and the global thread
11 identifier signal.

1 37. The apparatus of claim 36, wherein the plurality of signals comprises an
2 external pulse signal, an inverted external pulse signal, a scan clock signal,
3 and a local thread identifier signal.

1 38. The apparatus of claim 37, further comprising:
2 means for generating an internal pulse signal based on the behavior
3 of the clock signal;
4 means for using the internal pulse signal as a time reference for
5 operations;

6 means for using the internal pulse signal to generate the external
7 pulse signal; and
8 means for using the internal pulse to generate the inverted external
9 pulse signal.

1 39. The apparatus of claim 37, further comprising:
2 means for deactivating the external pulse signal when the global
3 thread identifier signal toggles;
4 means for reactivating the external pulse signal at an end of a cycle
5 in which the global thread identifier signal toggled; and
6 means for using the global thread identifier signal to generate the
7 local thread identifier signal.

1 40. The apparatus of claim 37, further comprising:
2 means for deactivating the external pulse signal when the multi-
3 function signal begins to serve as a scan enable function;
4 means for reactivating the external pulse signal dependent upon
5 whether the multi-function signal stopped serving as a scan
6 enable function before an end of a clock cycle in which the
7 multi-function signal began serving as the scan enable
8 function; and
9 means for activating a scan clock signal when the multi-function
10 signal serves as the scan enable function for more than one
11 clock cycle.

1 41. The apparatus of claim 36, further comprising:

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